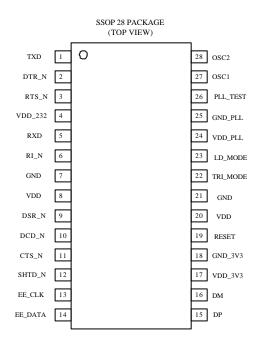


Data Sheet for PL2303 USB-to-RS232 Bridge

Features

- □ Full compliance with the USB Specification v1.1
- □ Support the RS232 Serial interface
- □ Support automatic handshake mode
- □ Over 1Mbps transfer rate
- □ Support remote wake-up and power management
- Dual data buffers for upstream and downstream data flow
- □ Support default ROM or external EEPROM for device configuration
- □ On chip USB transceiver
- □ On chip crystal oscillator running at 12M Hz
- □ 28 Pins SSOP package





1. Introduction

The PL-2303 operates as a bridge between one USB port and one standard RS232 Serial port. Figure 1 in the following page shows its interface and internal block diagram.

The two large on-chip buffers accommodate the data flow from two different buses. The USB bulk-type data is adopted for maximum data transfer. Automatic handshake is supported at the Serial port. With these, a much higher baud rate can be achieved compared to the legacy UART controller.

This device is also compliant with USB power management and remote wakeup scheme. Only minimum power is consumed from the host during suspend. By integrating all the functions into the SSOP-28 package, this chip is suitable for cable embedding. Users just simply hook the cable into PC or hub's USB port, then they can connect to any RS-232 devices.



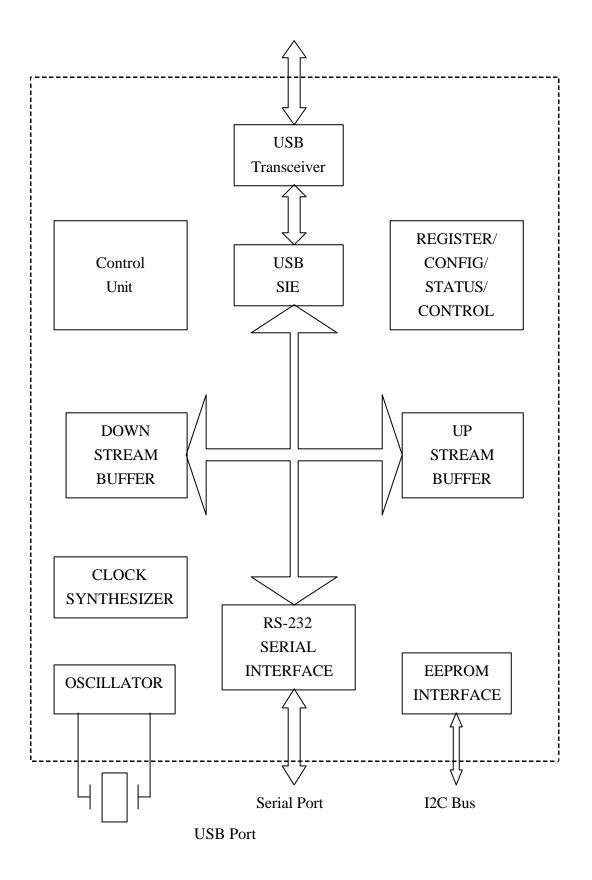




Figure 1. USB-Serial Block Diagram

2. Pin Description

I – Input signal	I* – 5V TTL Schmitt Input signal
O – Output signal	O* – 3.3V tri-state output
I/O – Bi-directional signal	P – Power/Ground

Table 1. Pins Description

Pin No.	Name	Туре	Description
1	TXD	0*	Data output to Serial port
2	DTR_N	O*	Data Terminal Ready, active low
3	RTS_N	0*	Request To Send, active low
4	VDD_232	Р	RS-232 VDD. The RS-232 output signals(Pin 1 ~ Pin
			3) are designed for 5V, 3.3V or 3V operation.
			VDD_232 should be connected to the same power
			level of the RS-232 interface. (The RS-232 input
			signals are always 5V~3V tolerant.)
5	RXD	I*	Data input from Serial Bus
6	RI_N	I*	Ring Indicator, active low
7	GND	Р	Ground
8	VDD	Р	Power
9	DSR_N	I*	Data Set Ready, active low
10	DCD_N	I*	Data Carrier Detect, active low
11	CTS_N	I*	Clear To Send, active low
12	SHTD_N	0	Shut Down RS232 Transceiver
13	EE_CLK	I/O	During Reset, this pin is input for simulation purpose.
			During normal operation, this pin is Serial ROM
1.4		T/O	clock
14	EE_DATA	I/O	Serial ROM data signal
15	DP	I/O	USB DPLUS signal
16	DM	I/O	USB DMINUS signal
17	VDD_3V3	0 D	3.3V power output from internal voltage regulator
18	GND_3V3	P	3.3V ground
19	RESET	I P	System Reset Power
20 21	VDD GND	P P	
			Ground
22	TRI_MODE	I	RS232 tri-state output control during Suspend
23	LD_MODE	Ι	Load Mode.
			At reset, LD_MODE is used to decide if this is a heavy load or light load device. High: indicates this is
			a 500 mA device. Low: indicates this is a 100 mA
			device.



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24	VDD_PLL	Р	5V power for PLL
25	GND_PLL	Р	Ground for PLL
26	PLL_TEST	Ι	PLL test mode control
27	OSC1	Ι	Crystal oscillator input
28	OSC2	Ο	Crystal oscillator output